STAND-ALONE/PARALLEL INTERFACE PRODUCTS

Basic Addressing

ISD single-chip voice record/playback devices include the capability of addressing multiple messages in a single chip. The address inputs provide the ability to partition the message space into a number of equal segments. They also provide access to the Operational Mode options of the device. The address inputs are positive logic and may be thought of as either binary or hex addressed. The binary convention is used in this manual.

Note that the address lines do not correspond to individual message numbers. One or more address lines must be HIGH and set to the correct *binary address* for a message to start anywhere in the memory.

The several series members have different sizes and addressing capability. Table 1 details these differences.

All the above devices are addressed in a similar manner. When addressing one of the 160 "message addresses" of the ISD1000A, for example, we are actually controlling a register in the device called the Message Start Pointer (MSP). The MSP points to where the next Record or Playback operation will begin. Usually, the address inputs pre-load the MSP when a chip enable or power-down initiated operation takes place. The Operational Mode Section will explain the exceptions.

Table 1: Array Size, Addresses, and Message Segments

Devices	Array Size	Binary Number of Add.	Actual Message Segments
ISD1100 Series	64K	256	80
ISD1200 Series	64K	256	80
ISD1400 Series	128K	256	160
ISD1000A Series	128K	256	160
ISD2532/40/48/64	256K	512	320
ISD2560/75/90/120	480K	1024	600

Table 2 shows the storage time, message resolution and the possible number of message addresses for the currently available ISD products.

To determine the value in the MSP, divide the message resolution of the device by the number of counts. For example, to start recording or playing back at the 4-second boundary of an ISD1016A, load the device with an address of 40 (when converted to binary, the actual physical address is 0010100).

Note that in addressing an ISD device, the address is how far "into" the message space MSP the is pointing. The address does not show how much time remains in the memory.

Table 2: Address Resolution

Device Part Number	Storage Time (seconds)	Msg. Resolution (msec)	Number of Message Addresses
ISD1016A	16	100	160
ISD1020A	20	125	160
ISD1110	10	125	80
ISD1112	12	150	80
ISD1210	10	125	80
ISD1212	12	150	80
ISD1416	16	100	160
ISD1420	20	125	160
ISD2532/60	32/60	100	320/600
ISD2540/75	40/75	125	320/600
ISD2548/90	48/90	150	320/600
ISD2564/120	64/120	200	320/600

NOTE: *Storage time and resolution subject to clock tolerances.*

Tables 2, 3, and 4 show example address boundaries for the ISD single-chip voice record/playback series products. They also show the address boundaries of unused space and the Operational Modes.

Message Addressing and Operational Mode Operations are mutually exclusive modes of the ISD devices. When Operational Mode is used, the MSP is always initialized to 0 (Unless an overriding Operational Mode is selected. See "Operational Modes" on under Application Information).

The ISD devices may be thought of as analog tape recorders with the capability of positioning the record/playback head anywhere on the tape at the address resolution given for each device. In the rest of this explanation on addressing, the ISD1016A will be used as the example. For a full list of all the ISD device address locations with time conversions for each device, see "Address Segment Resolution" under Application Information.

EXAMPLE OF RECORD AND PLAYBACK AT AN ADDRESS BOUNDARY

For this example, we are going to record a message starting at the 10 second boundary in an ISD1016A. Start by taking the PD pin to a LOW state and delaying T_{PUD} (see data sheet for the timing of the various ISD devices). An address of 100 (100 X .1 = 10 seconds) should be applied to the address pins. Converting 100 to binary we get the address of 01100100. Next take the P/$\overline{R}$ pin LOW. To begin record, take $\overline{CE}$ LOW and hold it in that state for the duration of the record time. When $\overline{CE}$ is taken back HIGH, the recording will end and an EOM bit is set in the EOM memory.

Table 3: ISD1100 and ISD1200 Address Space

Dec.	Binary								ISD1100/1200 (Seconds)
	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0.125
8	0	0	0	0	1	0	0	0	1.0
10	0	0	0	0	1	0	1	0	1.25
13	0	0	0	0	1	1	0	1	1.625
50	0	0	1	1	0	0	0	0	6.25
64	0	1	0	0	0	0	0	0	8.0
79	0	1	0	0	1	1	1	1	9.875

80	0	1	0	1	0	0	0	0
through	Unused address space. An ISD1100/1200 device addressed in this region will default to an overflow condition.							
191	1	0	1	1	1	1	1	1

192	1	1	0	0	0	0	0	0
through	This address space used by the ISD1100/1200 Operational Modes.							
255	1	1	1	1	1	1	1	1

To playback a message previously recorded at the 10-second boundary, the address pins are again loaded with an address of 100, and with PD LOW and P/$\overline{R}$ HIGH, $\overline{CE}$ is pulsed LOW. The ISD1016A will play back the message, stopping when it finds the set EOM bit. At the same time, the $\overline{EOM}$ pin will pulse LOW to indicate a message end. Whenever a Record operation is in progress and passes through the time of a previously set EOM bit, the bit is cleared. Thus, the EOM is recorded over and "erased."

SIMPLIFIED ADDRESSING SCHEMES

The ISD devices have eight, nine or ten address lines, depending upon which series is considered. For full control of the addressing this means that an 8- or 10-bit latch or microcontroller port must be used to completely address the ISD analog storage chip.

Table 4: ISD1000A and ISD1400 Address Space

Dec.	Binary								ISD1016A ISD1416 (Seconds)	ISD1020A ISD1420 (Seconds)
	A7	A6	A5	A4	A3	A2	A1	A0		
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0.1	0.125
8	0	0	0	0	1	0	0	0	0.8	1.0
10	0	0	0	0	1	0	1	0	1.0	1.25
13	0	0	0	0	1	0	0	0	1.3	1.625
50	0	0	1	1	0	0	1	0	5.0	6.25
100	0	1	1	0	0	1	0	0	10.0	12.5
159	1	0	0	1	1	1	1	1	15.9	19.875

160	1	0	1	0	0	0	0	0
through	Unused address space. An ISD1000A/1400 device addressed in this region will default to an overflow condition.							
191	1	0	1	1	1	1	1	1

192	1	1	0	0	0	0	0	0
through	This address space used by the ISD1000A/1400 Operational Modes.							
255	1	1	1	1	1	1	1	1

Table 5: ISD2500 Address Space

Dec.	Binary										ISD2560 (Seconds)	ISD2575 (Seconds)	ISD2590 (Seconds)	ISD25120 (Seconds)
	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0	0	0	0	1	1	0	0	1	0	5.0	6.25	7.5	10.0
100	0	0	0	1	1	0	0	1	0	0	10.0	12.5	15.0	20.0
250	0	0	1	1	1	1	1	0	1	0	25.0	31.25	37.5	50.0
300	0	1	0	0	1	0	1	1	0	0	30.0	37.5	45.0	60.0
400	0	1	1	0	0	1	0	0	0	0	40.0	50.0	60.0	80.0
500	0	1	1	1	1	1	0	1	0	0	50.0	62.5	75.0	100.0
599	1	0	0	1	0	1	0	1	1	1	59.9	74.875	89.85	119.8

600	1	0	0	1	0	1	1	0	0	0
through	Unused address space. An ISD2500 device addressed in this region will default to an overflow condition.									
767	1	0	1	1	1	1	1	1	1	1

768	1	1	0	0	0	0	0	0	0	0
through	This address space used by the ISD2500 Operational Modes.									
1023	1	1	1	1	1	1	1	1	1	1

Many product designs use small, inexpensive microcontroller chips and do not have sufficient port pins to handle the ISD device for full addressing. This need not be a serious obstacle. Most of these same applications do not need 100 ms. resolution of the address space. They can operate with less resolution. For each degree of resolution that is not used, one less port pin is needed. The following table (a simple binary count) illustrates this principle using an ISD1016A or ISD1416 as the example.

Table 6 indicates that by grounding the four least significant address bits, A0–A3, one can still address messages with a 1.6 second resolution using only four port or latch outputs. This would provide ten different 1.6-second message segments in an ISD1016A (ten 2-second messages in an ISD1020A) and might make it possible to use a smaller, less expensive microcontroller.

Table 6:   **ISD1016A or ISD1416 Address Resolution**

Address Line	No. of Address Lines	Address Resolution (sec)
A0	8	0.1
A1	7	0.2
A2	6	0.4
A3	5	0.8
A4	4	1.6
A5	3	3.2
A6	2	6.4
A7	1	12.8

By some study of the addressing scheme many different combinations of simplified addressing can be developed. Another example is to have four 2.5-second messages in an ISD1110 or ISD1210 device by using only two address lines from the controller.

Table 7:   **ISD1110 or ISD1210 Four Message Approach**

Msg #	Addr	A7	A6	A5	A4	A3	A2	A1	A0
1	000	0	0	0	0	0	0	0	0
2	020	0	0	0	1	0	1	0	0
3	040	0	0	1	0	1	0	0	0
4	060	0	0	1	1	1	1	0	0
				L1	L0	L1	L0		

Address lines A0, A1, A6, and A7 are all tied to ground. Address line A2 is tied to A4 (this is now L0) and A3 is tied to A5 (this is now L1). Then, Table 8 becomes a simple 2-bit binary count that requires only the two port lines (L0, L1) for four 2.5-second messages.

Table 8:   **Two-line Select**

Msg #	Addr.	L1	L0
1	000	0	0
2	020	0	1
3	040	1	0
4	060	1	1

For the ISD2560/75/90/120 series of devices there are ten address lines that can be used for the 100-msec resolution. As with the other devices, this can be greatly simplified to reduce addressing lines needed. The following table compares the tradeoffs between the number of address lines used, the number of messages possible and the size of those messages derived.

Table 9:   **ISD2560 Addressing**

Lines Used	# of Msgs.	Msg Size (Sec.)	Notes
4	9	6.4	Last msg. = 8.8 sec.
6	7	8.0	Last msg. = 12 sec.
7	8	7.2	Last msg. = 9.6 sec.
7	6	10.0	Exact fit
8	8	7.6	Last msg. = 6.8 sec.

Similar techniques work for the ISD2575, the difference being the timing or message size.

Table 10:   **ISD2575 Addressing**

Lines Used	# of Msgs.	Msg Size (Sec)	Notes
4	9	8.0	Last msg. = 11 sec.
5	18	4.0	Last msg. = 7 sec.
6	12	6.0	Last msg. = 9 sec.
8	10	7.5	Exact fit